

If the values have not converged, then blocks 32-37 can be repeated using the calculated times rather than the assumed simultaneous times in block 42 of FIG. 7. Such an iteration will improve the accuracy of the simulations. Although the entirety of blocks 32-37 and the corresponding blocks of FIGS. 7 and 8 may be repeated, this may be undesirable and unnecessary. A more streamlined approach would be to asses each of the plurality of local clock nets in a top down manner to determine whether to re-run the simulation for each particular local clock net. Similar to above, the simulations may be re-run in parallel. All of the local clock nets are reviewed and re-run in block 32 before the global clock net is re-run in block 34. It may not be necessary to re-run the global clock net simulation if the re-calculated loads of the local clock nets attached directly to the global clock net have not changed substantially, that is, they have not changed enough to affect the clock arrival times of the global clock net. As the various simulations are re-run, the CDM is updated. In an effort to further streamline the iteration process, it is possible to skip blocks 38 and 40 of FIG. 7 as this information is already stored in the CDM and has not changed. Also, it is possible to skip blocks 46 and 48 of FIG. 8 for the same reason. Eventually through the iteration process the results will converge and the process will end leaving a substantially fully developed simulation and CDM.--

IN THE CLAIMS:

Please amend claims 1, 7-10, 15, 20, 21 and 26 as follows:

1. (Once Amended) A Clock Data Model (CDM) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising:

partitioning a complete clock net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form a complete clock net simulation; and storing the plurality of simulations in the Clock Data Model.

7. (Once Amended) The CDM as defined in claim 6, wherein clock arrival times from the global clock net at all points where a given local clock net is connected to the global clock net are assumed to occur simultaneously when the given local clock net is being simulated.

8. (Once Amended) The CDM as defined in claim 1, wherein simulating the global clock net comprises:

extracting the layout of the global clock net from a microprocessor network database;

extracting component values of the elements of the global clock net from the microprocessor network database;

extracting the simulated loads of the plurality of local clock nets from the CDM; and

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

9. (Once Amended) The CDM as defined in claim 1, wherein the method further comprises evaluating the complete clock net simulation to determine whether results of the simulations converge.

10. (Once Amended) The CDM as defined in claim 9, wherein, if the results do not converge, the method further comprises:

re-simulating the at least one of the plurality of local clock nets using a corresponding calculated clock arrival time, to generate a load for the at least one local clock net on the global clock net;

re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

combining the simulations and re-simulations to form the complete clock net simulation.

15. (Once Amended) A Clock Data Model (CDM) for use with a system for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the system comprising means for partitioning a complete clock net into a global clock net and a plurality of local clock nets, means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, means for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets, and means for combining the plurality of simulations to form a complete clock net simulation, the CDM comprising:

means for storing the plurality of simulation results.

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20. (Once Amended) The CDM as defined in claim 15, wherein the system further comprises means for evaluating the complete clock net to determine whether the results converge, means for assuming that clock arrival times are those calculated for the simulated global clock net, means for re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, means for re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets, and means for combining the simulations and re-simulations to form the complete clock net simulation and wherein the CDM further comprises means for storing the plurality of re-simulation results.

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21. (Once Amended) A Clock Data Model (CDM) for use with a system for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the system comprising a partitioner for horizontally and vertically partitioning a complete clock net into a global clock net and a plurality of local clock nets, at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, a global clock net simulator for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets, and a merging unit for combining the plurality of simulations to form a complete clock net simulation, the CDM comprising:

a memory for storing the plurality of simulation results.

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26. (Once Amended) The CDM as defined in claim 21, wherein the system further comprises a convergence evaluator for evaluating the complete clock net to determine whether

the results converge and, when the results are found not to converge, the system assumes that clock arrival times are those calculated for the simulated global clock net, the at least one local clock net simulator re-simulates at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, the global clock net simulator re-simulates the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets, and the merging unit combines the simulations and re-simulations to form the complete clock net simulation and wherein the CDM further comprises a memory for storing the plurality of re-simulation results.